FORM PTO-1390 U S DEPARTMENT OF COMMERCE PATENT AND TRADEMARK OFFICE

TRANSMITTAL LETTER TO THE UNITED STATES DESIGNATED/ELECTED OFFICE (DO/EO/US) CONCERNING A FILING UNDER 35 U.S.C. 371

ATTORNEY'S DOCKET NUMBER: 60188-131

U.S. APPLIC. NO. (if known, see 37 CFR 1.5): 10/009842

INTERNATIONAL APPLICATION NO.	INTERNATIONAL FILING DATE	PRIORITY DATE CLAIMED
PCT/JP00/03884	June 14, 2000	June 16, 1999

TITLE OF INVENTION

SEMICONDUCTOR DEVICE

APPLICANTS FOR DO/EO/US

Kyoko HIRATA and Hiroshi SHIMOMURA

Applicant herewith submits to the United States Designated/Elected Office (DO/EO/US) the following items and other information:

1. ☒ This is a **FIRST** submission of items concerning a filing under 35 U.S.C. 371.

2. ☐ This is a **SECOND** or **SUBSEQUENT** submission of items concerning a filing under 35 U.S.C. 371.

3. ☒ This express request to begin national examination procedures (35 U.S.C. 371(f)) at any time rather than delay examination until the expiration of the applicable time limit set in 35 U.S.C. 371(b) and PCT Articles 22 and 39(1).

4. ☒ A proper Demand for International Preliminary Examination was made by the 19th month from the earliest claimed priority date.

5. ☒ A copy of the International Application as filed (35 U.S.C. 371(c)(2))
   a. ☐ is transmitted herewith (required only if not transmitted by the International Bureau).
   b. ☒ has been transmitted by the International Bureau.
   c. ☐ is not required, as the application was filed in the United States Receiving Office (RO/US)

6. ☒ A translation of the International Application into English (35 U.S.C. 371(c)(2)).

7. ☐ Amendments to the claims of the International Application under PCT Article 19 (35 U.S.C. 371(c)(3))
   a. ☐ are transmitted herewith (required only if not transmitted by the International Bureau).
   b. ☐ have been transmitted by the International Bureau.
   c. ☐ have not been made; however, the time limit for making such amendment has NOT expired.
   d. ☐ have not been made and will not be made.

8. ☐ A translation of the amendments to the claims under PCT Article 19 (35 U.S.C. 371(c)(3)).

9. ☒ An oath or declaration of the inventor(s) (35 U.S.C. 371(c)(4)).

10. ☐ A translation of the annexes to the International Preliminary Examination Report under PCT Article 36 (35 U.S.C. 371(c)(5)).

Items 11. to 16. below concern other document(s) or information included:

11. ☒ An Information Disclosure Statement under 37 CFR 1.97 and 1.98.

12. ☒ An assignment document for recording. A separate cover sheet in compliance with 37 CFR 3.28 and 3.31 is included.

13. ☒ A FIRST preliminary amendment.
    ☐ A SECOND or SUBSEQUENT preliminary amendment.

14. ☐ A substitute specification.

15. ☐ A change of power of attorney and/or address letter.

16. ☒ Other items or information.
    1. International Search Report prepared by JPO.
    2. Front page of Published International Application.
    3. International Preliminary Examination Report.
    4. PCT Demand.
    5. PCT/IB/301,304,308 & 332.
    6. Amendments to claims.
    7. Associate Power of Attorney.

U.S. APPLIC. NO. (if known, see 37 CFR 1.50)	INTERNATIONAL APPLICATION NO.	ATTORNEY'S DOCKET NUMBER
10/009842	PCT/JP00/03884	60188-131

	CALCULATIONS	PTO USE ONLY

17. ☒ The following fees are submitted:

Basic National Fee (37 CFR 1.492(a)(1)-(5)): Search Report has been prepared by the EPO or JPO	$890.00
International preliminary examination fee paid to USPTO (37 CFR 1.482)	$710.00
No international preliminary examination fee paid to USPTO (37 CFR 1.482) but international search fee paid to USPTO (37 CFR 1.445(a)(2))	$740.00
Neither international preliminary examination fee (37 CFR 1.482) nor international search fee (37 CFR 1.445(a)(2)) paid to USPTO	$1,040.00
International preliminary examination fee paid to USPTO (37 CFR 1.482) and all claims satisfied provisions of PCT Article 33(2)-(4)	$100.00

ENTER APPROPRIATE BASIC FEE AMOUNT =	$ 890.00	
Surcharge of $130.00 for furnishing the oath or declaration later than ☐ 20 ☐ 30 months from the earliest claimed priority date (37 CFR 1.492(e)).	$ 0.00	

Claims	Number Filed	Number Extra	Rate		
Total Claims	13 -20 =	0	x $18.00	$0.00	
Independent Claims	1 -3 =		x $84.00	$ 0.00	
Multiple dependent claim(s) (if applicable)			+ $280.00	$ 0.00	
TOTAL OF ABOVE CALCULATIONS =				$890.00	
Reduction by 1/2 for filing by small entity, if applicable. Verified Small Entity Statement must also be filed. (Note 37 CFR 1.9, 1.27, 1.28).				$ 0.00	
SUBTOTAL =				$ 890.00	
Processing fee of $130.00 for furnishing the English translation later than the ☐ 20 ☐ 30 months from the earliest claimed priority date (37 CFR 1.492(f)).			+	$ 0.00	
TOTAL NATIONAL FEE =				$ 890.00	
Fee for recording the enclosed assignment (37 CFR 1.21(h)). The assignment must be accompanied by an appropriate cover sheet (37 CFR 3.28, 3.31). $40.00 per property			+	$ 40.00	
TOTAL FEES ENCLOSED =				$930.00	
				Amount to be: refunded	$
				charged	$ 930.00

a. ☐ A check in the amount of $ _____ to cover the above fees is enclosed.

b. ☒ Please charge my Deposit Account No. 500417 in the amount of $ 930.00 to cover the above fees. A duplicate copy of this sheet is enclosed.

c. ☒ The Commissioner is hereby authorized to charge any additional fees which may be required, or credit any overpayment to Deposit Account No. 500417. A duplicate copy of this sheet is enclosed.

NOTE: Where an appropriate time limit under 37 CFR 1.494 or 1.495 has not been met, a petition to revive (37 CFR 1.137(a) or (b)) must be filed and granted to restore the application to pending status.

SEND ALL CORRESPONDENCE TO:

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SIGNATURE
Michael E. Fogarty
NAME
36,139
REGISTRATION NUMBER
December 17, 2001

Docket No.: 60188-131 PATENT

IN THE UNITED STATES PATENT AND TRADEMARK OFFICE

In re Application of	:	
Kyoko HIRATA, et al.	:	
Serial No.:	:	Group Art Unit:
Filed: December 17, 2001	:	Examiner:
For: SEMICONDUCTOR DEVICE	:	

PRELIMINARY AMENDMENT

Commissioner for Patents
Washington, DC 20231

Sir:

Prior to examination of the above-referenced application, please amend the application as follows:

IN THE SPECIFICATION:

Please replace the paragraph beginning at page 30, line 21, continuing on to page 31, with the following rewritten paragraph:

--FIG. **14(a)** is a schematic top view showing a diode element **500** included in a semiconductor device of this embodiment, and FIG. **14(b)** is a schematic cross-sectional view of the diode element **500** taken along line **b-b'** of FIG. **14(a).** The diode element **500** includes a first unit cell **10** in a first conductive type semiconductor layer (N-well) **30** and a plurality of second unit cells **20** formed in the first unit cell **10**. In this embodiment, the first unit cell **10** viewed from the normal line direction of the substrate is for example, square in shape (the length

of each side: about 25μm), and the second unit cells **20** are also square in shape (the length of each side: about 5μm). For example, four second unit cells **20** are formed in the first unit cell **10**. A spacing **15** between the first unit cell **10** and the second unit cells **20** is for example, about 2μm.--

IN THE CLAIMS:

Please amend the claims as follows:

3. (Amended) The semiconductor device according to claim 1, wherein a dimension that defines a size of each of the first semiconductor region and the second semiconductor region is substantially a same as a minimum dimension that is allowed by a design rule for the semiconductor device.

4. (Amended) The semiconductor device according to claim 1, wherein each of the first semiconductor region and the second semiconductor region viewed from a normal line direction is substantially square in shape.

5. (Amended) The semiconductor device according to claim 1, wherein the first unit cells and the second unit cells are arranged in a checkered pattern in the first conductive type semiconductor layer.

6. (Amended) The semiconductor device according to claim 1, wherein the first unit cell and the second unit cell are arranged in the first conductive type semiconductor layer with a predetermined distance to each other, and on an intercell region that is positioned between the first unit cell and the second unit cell in the first conductive type semiconductor layer, a gate electrode structure including at least an insulating layer formed on the cell region and a conductive layer formed on the insulating layer is formed.

9. (Amended) The semiconductor device according to claim 1, further comprising a second conductive type semiconductor layer, wherein the first conductive type semiconductor layer is formed on the second conductive type semiconductor layer.

11. (Amended) The semiconductor device according to claim 9, wherein the second conductive type semiconductor layer is a semiconductor substrate, and the first conductive type semiconductor layer is a well region formed in the semiconductor substrate.

12. (Amended) The semiconductor device according to claim 1, wherein the first conductive type semiconductor layer is formed on an insulating layer.

13. (Amended) The semiconductor device according to claim 1, further comprising an analog circuit section and a digital circuit section, wherein the diode element is formed in the

analog circuit section, and the analog circuit section and the digital circuit section are produced

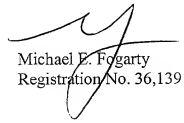
by a CMOS process.

REMARKS

The above-referenced application is amended to delete the multiple dependency of claims 3-6, 9 and 11-13 to avoid the multiple dependent claim filing fee and to make changes to the specification. Attached hereto is a marked-up version of the changes made. Entry of this preliminary amendment is respectfully requested.

Respectfully submitted,

MCDERMOTT, WILL & EMERY



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MARKED-UP VERSION OF AMENDMENTS

IN THE SPECIFICATION:

The paragraph beginning at page 30, line 21, continuing on to page 31, has been amended as follows:

FIG. **14(a)** is a schematic top view showing a diode element **500** included in a semiconductor device of this embodiment, and FIG. **14(b)** is a schematic cross-sectional view of the diode element **500** taken along line **b-b'** of FIG. **14(a)**. The diode element **500** includes a first unit cell **10** in a first conductive type semiconductor layer (N-well) **30** and a plurality of second unit cells **20** formed in the first unit cell **10**. In this embodiment, the first unit cell **10** viewed from the normal line direction of the substrate is for example, square in shape (the length of each side: about 25[5] μm), and the second unit cells **20** are also square in shape (the length of each side: about 5 [25] μm). For example, four second unit cells **20** are formed in the first unit cell **10**. A spacing **15** between the first unit cell **10** and the second unit cells **20** is for example, about 2μm.

The claims have been amended as follows:

3. (Amended) The semiconductor device according to claim 1 [or 2], wherein a dimension that defines a size of each of the first semiconductor region and the second semiconductor region is substantially a same as a minimum dimension that is allowed by a design rule for the semiconductor device.

4. (Amended) The semiconductor device according to claim 1 [any of claims 1 to 3], wherein each of the first semiconductor region and the second semiconductor region viewed from a normal line direction is substantially square in shape.

5. (Amended) The semiconductor device according to claim 1 [any of claims 1 to 4], wherein the first unit cells and the second unit cells are arranged in a checkered pattern in the first conductive type semiconductor layer.

6. (Amended) The semiconductor device according to claim 1 [any of claims 1 to 5], wherein the first unit cell and the second unit cell are arranged in the first conductive type semiconductor layer with a predetermined distance to each other, and on an intercell region that is positioned between the first unit cell and the second unit cell in the first conductive type semiconductor layer, a gate electrode structure including at least an insulating layer formed on the cell region and a conductive layer formed on the insulating layer is formed.

9. (Amended) The semiconductor device according to claim 1 [any of claims 1 to 8], further comprising a second conductive type semiconductor layer, wherein the first conductive type semiconductor layer is formed on the second conductive type semiconductor layer.

11. (Amended) The semiconductor device according to claim 9 [or 10], wherein the second conductive type semiconductor layer is a semiconductor substrate, and the first conductive type

semiconductor layer is a well region formed in the semiconductor substrate.

12. (Amended) The semiconductor device according to claim 1 [any of claims 1 to 8], wherein the first conductive type semiconductor layer is formed on an insulating layer.

13. (Amended) The semiconductor device according to claim 1 [any of claims 1 to 12], further comprising an analog circuit section and a digital circuit section, wherein the diode element is formed in the analog circuit section, and the analog circuit section and the digital circuit section are produced by a CMOS process.

13/PRTS

DESCRIPTION

SEMICONDUCTOR DEVICE

Technical Field

The present invention relates to a semiconductor device, in particular, a semiconductor device including a high-performance diode element that occupies only a small area.

Background Art

In recent years, with the development of a system LSI directed to a one-chip solution, the importance of an analog CMOS circuit in which an analog circuit is realized by the production process of a CMOS circuit (complementary electric-field transistor circuit) has been increased. In the system LSI by the CMOS process, the performance of the LSI often depends on the performance of the analog CMOS circuit, and thus it is very important to design a high-performance analog circuit. When designing a high-performance analog circuit, it is necessary to provide a reference voltage circuit or a reference current circuit in order to eliminate influences such as noise from a digital circuit block or fluctuations of a power supply voltage as much as possible. Moreover, in order to reduce power consumption or to match different voltages between a circuit for protecting an internal circuit from external noise and

the internal circuit with each other, it is also necessary to provide a voltage converter circuit or the like.

When a reference voltage circuit that is required to design a high-performance analog circuit is constituted with a Zener diode, the power supply voltage increases and the problem that noise is generated in the circuit occurs. Thus, instead of the reference voltage circuit using a Zener diode, a reference voltage circuit using a bandgap reference has been utilized in the LSI. In the case of a CMOS LSI, a bandgap reference circuit including a diode utilizing a pn junction of a MOS transistor has been used in view of both the production cost and the fact that it can be realized by using the same process as that for a digital circuit block. In order to improve the precision of the analog circuit in the system LSI, it is necessary to improve the precision of the bandgap reference circuit utilizing a diode. To achieve this, it is indispensable to develop a diode having excellent characteristics.

On the other hand, with a demand for reduction in the chip area of the LSI, reduction in the chip area of the system LSI is also in demand and miniaturization of an analog/digital mixed LSI is in progress. However, unlike a digital circuit section that can be comparatively easily miniaturized, in the case of an analog circuit section, it is difficult to reduce the area of the analog circuit section because it is necessary to consider non-uniformity, temperature dependency and the like. In order to reduce the

chip area of the analog/digital mixed LSI, how much the analog circuit section area can be reduced is an important point. Therefore, it is important to reduce the area that a diode element provided in the analog circuit section occupies.

The inventors of the present invention examined the structure of a diode element **1000** as shown in FIG. **15**. FIG. **15(a)** is a schematic top view showing the diode element **1000**, and FIG. **15(b)** is a schematic cross-sectional view of the diode element **1000** taken along line **b-b'** of FIG. **15(a)**.

The diode element **1000** has a structure that can be comparatively easily produced by using the CMOS process, and includes a P^+ diffusion region **122** formed in the center of an N-well region (NW) **130**, an element isolation region oxide film (an oxide film for isolating the elements) **132** surrounding the outer circumference of the P^+ diffusion region **122**, and an N^+ diffusion region **112** surrounding the outer circumference of the element isolation region oxide film **132**. A P-well region (PW) **136** is formed around the N-well region **130** and a P^+ diffusion region **134** is formed in the P-well region (PW) **136** so as to enclose the element isolation region oxide film **132** that is positioned around the N^+ diffusion region **112**.

The P^+ diffusion region **122** and the N^+ diffusion region **112** are formed in the N-well region **130**, and a pn junction is formed on a junction face between the P^+ diffusion region **122** and the N-well region **130**. Therefore, a diode can be

constituted by using the P^+ diffusion region **122** as an anode and the N^+ diffusion region **112** as a cathode. In the diode element **1000**, one diode includes a junction of a pair of p and n, and therefore as the pn junction area (i.e., the bottom area of the P^+ diffusion region **122**) increases, the current capacity of the diode element **1000** increases. Unlike the N^+ diffusion region **112** or the P^+ diffusion region **122** that have comparatively low electrical resistances, the N-well region **130** has a comparatively high electrical resistance, and thus a parasitic resistance **140** exists in the N-well region **130**. This parasitic resistance **140** is connected in series to the diode constituted by the pn junction between the P^+ diffusion region **122** and the N-well region **130**. Thus, the parasitic resistance **140** of the N-well region **130** causes a voltage drop of the diode. As a result, the current capacity of the diode element **1000** is decreased. Therefore, in order to design the diode element **1000** such that a desired current capacity can be obtained, a layout is designed after determining a P^+ diffusion region size **124** that defines the bottom area of the P^+ diffusion region **122** and a distance (a distance between the P^+ diffusion region **122** and the N^+ diffusion region **112**) **114** that defines the magnitude of the parasitic resistance **130**.

However, when the diode element **1000** is designed so as to have a higher current capacity, it is necessary to increase the size of the P^+ diffusion region **122** that is positioned in the center of the N-well region **130**, and thus

the distance from the center of the P^+ diffusion region **122** to the N^+ diffusion region **112** increases. As a result, the parasitic resistance **140** of the N-well region **130** increases. Since the parasitic resistance **140** decreases the current capacity of the diode element **1000**, further increase in the size of the P^+ diffusion region **122** is required in order to obtain a desired current capacity, and as a result, reduction in the chip area is inhibited. Furthermore, the parasitic resistance **140** decreases the current capacity of the diode element **1000** more increasingly with increasing diode current (ID). Therefore, this phenomenon is a problem particularly when a comparatively high current flows through the diode element **1000** with a certain P^+ diffusion region size **124**.

The present invention is carried out in view of the above, and has a main object of providing a semiconductor device including a high-performance diode element that occupies only a small area.

Disclosure of Invention

A semiconductor device of the present invention includes a first conductive type semiconductor layer; at least one first unit cell including a first conductive type first semiconductor region formed in the first conductive type semiconductor layer and a contact region for electrically connecting the first semiconductor region to a line; and at least one second unit cell including a second

conductive type second semiconductor region formed in the first conductive type semiconductor layer and a contact region for electrically connecting the second semiconductor region to a line, and the first unit cell and the second unit cell act as a diode element in cooperation.

It is preferable that the at least one first unit cell is a plurality of first unit cells and the at least one second unit cell is a plurality of second unit cells.

It is preferable that a dimension that defines a size of each of the first semiconductor region and the second semiconductor region is substantially the same as the minimum dimension that is allowed by a design rule for the semiconductor device.

It is preferable that each of the first semiconductor region and the second semiconductor region viewed from a normal line direction is substantially square in shape.

It is preferable that the first unit cell and the second unit cell are arranged in a checkered pattern in the first conductive type semiconductor layer.

In an embodiment, the first unit cell and the second unit cell are arranged in the well region with a predetermined distance to each other, and on an intercell region that is positioned between the first unit cell and the second unit cell in the first conductive type semiconductor layer, a gate electrode structure having at least an insulating layer formed on the cell region and a conductive layer formed on the insulating layer is formed.

In an embodiment, the present invention further includes a gate line electrically connected to the gate electrode structure.

In an embodiment, a plurality of second unit cells are formed in the first semiconductor region of one first unit cell.

In an embodiment, the present invention further includes a second conductive type semiconductor layer, and the first conductive type semiconductor layer is formed on the second conductive type semiconductor layer.

In an embodiment, the first unit cell formed in the first conductive type semiconductor layer is used as a base, the second unit cell is used as an emitter, and the second conductive type semiconductor is used as a collector.

In an embodiment, the second conductive type semiconductor layer is a semiconductor substrate, and the first conductive type semiconductor layer is a well region formed in the semiconductor substrate.

In an embodiment, the first conductive type semiconductor layer is formed on the insulating layer.

In an embodiment, the present invention further includes an analog circuit section and a digital circuit section, and the diode element is formed in the analog circuit section, and the analog circuit section and the digital circuit section are produced by a CMOS process.

The present invention is provided with a first unit cell and a second unit cell, and the first unit cell and the

second unit cell constitute a diode element. Thus, a first conductive type first semiconductor region of the first unit cell and a second conductive type second semiconductor region of the second unit cell can be arranged in close proximity to each other, so that the distance between the anode and the cathode can be decreased. As a result, the parasitic resistance of the first conductive type semiconductor layer can be reduced, which makes it possible to provide a semiconductor device including a high-performance diode element that occupies only a small area. When a plurality of first unit cells and a plurality of second unit cells are provided, the current capacity of the diode element can be increased by increasing the area of the pn junctions.

Moreover, when the dimension that defines the size of each of the first semiconductor region and the second semiconductor region is substantially the same as the minimum dimension that is allowed by a design rule, the distance between the anode and the cathode can be decreased more effectively, and thus the parasitic resistance can be reduced effectively. Furthermore, the size of the diode element can be minimized, and as a result, the chip area of the semiconductor device can be reduced. When each of the first semiconductor region and the second semiconductor region is substantially square in shape, the first unit cells and the second unit cells can be arranged most efficiently under the predetermined design rule. Moreover,

when the first unit cells and the second unit cells are arranged in a checkered pattern, the parasitic resistance of the first conductive type semiconductor layer can be reduced more effectively.

When a gate electrode structure is formed on an intercell region between the first unit cell and the second unit cell, it is unnecessary to provide an element isolation region oxide film between the first unit cell and the second unit cell, so that an outer circumferential face of the second unit cell can be used as a pn junction face. Thus, the area of pn junctions can be further increased without increasing the element area of the diode element. When a gate line that is electrically connected to the gate electrode structure is further formed, the characteristics of the diode element can be altered by applying an independent voltage to the gate line.

Even in a structure in which a plurality of second unit cells are formed in the first semiconductor region of one first unit cell, the distance between the anode and the cathode can be decreased, so that the parasitic resistance of the first conductive type semiconductor layer can be reduced. The first conductive type semiconductor layer is for example, formed on the second conductive type semiconductor layer. In the case of this structure, with the first unit cell as a base, the second unit cell as an emitter and the second conductive type semiconductor layer as a collector, a bipolar transistor element can be

constituted by using the first unit cell and the second unit cell. Also in this structure, a bipolar transistor element having an improved current capacity can be provided because the parasitic resistance of the first conductive type semiconductor layer is reduced. The first conductive type semiconductor layer can be a well region formed in a semiconductor substrate. Moreover, the first conductive type semiconductor layer can be also formed on an insulating layer (or an insulating substrate). The diode element including the first unit cell and the second unit cell is for example, formed in an analog circuit section and preferably has a structure that can be produced, using the CMOS process.

Brief Description of Drawings

FIG. **1(a)** is a schematic top view showing a diode element **100** included in a semiconductor device of Embodiment **1**, and FIG. **1(b)** is a cross-sectional view of the diode element **100** taken along line **b-b'** of FIG. **1(a)**.

FIGS. **2(a)** to **2(e)** are cross-sectional views of a process sequence for illustrating a method for producing the diode element **100**.

FIG. **3(a)** is a schematic top view of a diode element **200** included in the semiconductor device of Embodiment **1**, and FIG. **3(b)** is a cross-sectional view of the diode element **200** taken along line **b-b'** of FIG. **3(a)**.

FIGS. **4(a)** to **4(f)** are cross-sectional views of a

process sequence for illustrating a method for producing the diode element **200**.

FIG. **5** is a circuit diagram for voltage/current characteristics of a diode.

FIG. **6** is a graph showing the measurement results of voltage/current characteristics of the diode measured with the circuit shown in FIG. **5**.

FIG. **7** is a graph showing an enlarged portion where an applied voltage is around 0.7V in the graph of FIG. **6**.

FIG. **8** is a graph showing the range of 0.6V to 1.0V as the applied voltage in the graph of FIG. **6**.

FIG. **9(a)** is a schematic top view showing a diode element **300** included in a semiconductor device of Embodiment **2**, and FIG. **9(b)** is a schematic cross-sectional view of the diode element **300** taken along line **b-b'** of FIG. **9(a)**.

FIGS. **10(a)** to **10(f)** are cross-sectional views of a process sequence for illustrating a method for producing the diode element **300**.

FIG. **11(a)** is a schematic top view showing a bipolar transistor element **400** included in a semiconductor device of Embodiment **3**, and FIG. **11(b)** is a schematic cross-sectional view of the bipolar transistor element **400** taken along line **b-b'** of FIG. **11(a)**.

FIG. **12** is another schematic cross-sectional view showing the bipolar transistor element **400**.

FIG. **13** is a schematic cross-sectional view showing a bipolar transistor element **450**.

FIG. **14(a)** is a schematic top view showing a diode element **500** included in a semiconductor device of Embodiment **4**, and FIG. **14(b)** is a schematic cross-sectional view of the diode element **500** taken along line **b-b'** of FIG. **14(a)**.

FIG. **15(a)** is a schematic top view showing a diode element **1000**, and FIG. **15(b)** is a schematic cross-sectional view of the diode element **1000** taken along line **b-b'** of FIG. **15(a)**.

Best Mode for Carrying Out the Invention

Hereinafter, embodiments of the present invention will be described with reference to the accompanying drawings. In the following drawings, for simplification, elements having substantially the same function bear the same reference numerals.

(Embodiment **1**)

Hereinafter, Embodiment **1** of the present invention will be described with reference to FIGS. **1** to **6**. A semiconductor device of this embodiment is a device including a semiconductor integrated circuit and, for example, is an analog/digital mixed LSI produced by a CMOS process. The semiconductor device of this embodiment includes a diode element **100** shown in FIG. **1** in the semiconductor integrated circuit. FIG. **1(a)** is a schematic top view showing the diode element **100**, and FIG. **1(b)** is a schematic cross-sectional view of the diode element **100**

taken along line **b-b'** of FIG. **1(a)**.

The diode element **100** has a first conductive type semiconductor layer **30**, and first unit cells **10** and second unit cells **20** formed in the first conductive type semiconductor layer **30**. The first conductive type semiconductor layer **30** is for example, an N-well region (NW) **30** formed in a P-type semiconductor substrate **60**. The first conductive type semiconductor layer **30** is not limited to the first conductive type well region, but may be, for example, a first conductive type semiconductor substrate or a first conductive type semiconductor layer formed on a second conductive type semiconductor substrate. Moreover, in this embodiment, the N-well region **30** is used as the first conductive type semiconductor layer, but it can be replaced by a P-well region.

The first unit cell **10** has a first conductive type first semiconductor region **12** formed in the N-well region **30** and a contact region **14** for electrically connecting the first semiconductor region **12** to a line **50**. In this embodiment, the first conductive type first semiconductor region **12** is an N^+ diffusion region, and the N^+ diffusion region **12** is electrically connected to the line **50** through a contact section **52** joined to the contact region **14** provided on the surface thereof. On the other hand, the second unit cell **20** has a second conductive type second semiconductor region **22** formed in the N-well region **30** and a contact region **24** for electrically connecting the first

semiconductor region **10** to the line **50**. In this embodiment, the second conductive type second semiconductor region **22** is a P^+ diffusion region, and the P^+ diffusion region **22** is electrically connected to the line **50** through the contact section **52** joined to the contact region **24** provided on the surface thereof. When a P-well region is formed as a first conductive type semiconductor layer, the first conductive type first semiconductor region **12** can be used as the P^+ diffusion region and the second conductive type second semiconductor region **12** can be used as the N^+ diffusion region.

In this embodiment, the first unit cell **10** and the second unit cell **20** are arranged with a predetermined distance (e.g., about 2μm) to each another. In order to separate the first unit cell **10** (N^+ diffusion region **12**) and the second unit cell **20** (P^+ diffusion region),an element isolation region oxide film (a field oxide film) **32** is formed in an intercell region (an element isolation region) between the first unit cell **10** and the second unit cell **20** in the N-well region **30**. Moreover, a P-well region (PW) **36** is formed around the N-well region **30**, and a P^+ diffusion region **34** is formed in the P-well region **36** so as to surround the outer circumference of the element isolation region oxide film **32** that separates the first unit cell **10** and the second unit cell **20**.

The N^+ diffusion region **12** of the first unit cell **10** and the P^+ diffusion region **22** of the second unit cell **20**

are formed in the N-well region **30**, and the P^+ diffusion region **22** forms a pn junction with the N-well region **30**. Thus, the function as a diode can be realized by using the second unit cell **20** (the P^+ diffusion region **22**) as an anode and the first unit cell **10** (the N^+ diffusion region **12**) as a cathode.

In the diode element **100** of this embodiment, unlike the above-described diode element **1000**, the first unit cell **10** and the second unit cell **20** constitute a diode, so that the distance between the anode and the cathode is shorter than that of the diode element **1000**. Thus, a parasitic resistance **40** present in the N-well region **30** can be reduced more significantly than in the structure of the diode element **1000**. In other words, since the first unit cell **10** and the second unit cell **20** can be laid out in the N-well region **30** so as to be in close proximity to each other, current flows through the N-well region **30** where the parasitic resistance **40** exists in a shorter distance. As a result, the parasitic resistance **40** can be reduced. When the parasitic resistance **40** is reduced, a significant decrease of the current capacity of the diode element **100** can be prevented even if the diode current (ID) is increased, and therefore a semiconductor device provided with the high-performance diode element **100** having a high current capacity per unit area can be provided. Moreover, since the diode element **100** has a higher current capacity per unit area than the diode element **1000**, it can be formed in a smaller area.

In this embodiment, a plurality of first unit cells **10** and a plurality of second unit cells **20** are formed in the N-well region **30**. Thus, the current capacity of the diode element can be increased by increasing the pn junction area. In an example shown in FIG. **1**, four first unit cells **10** and five second unit cells **20** are arranged two-dimensionally (in a matrix form), but not limited thereto. It is also possible to provide a larger number of first unit cells **10** and second unit cells **20**. Moreover, the line **50** may not be connected to all of the plurality of first unit cells **10** and all of the plurality of second unit cells **20**. The line **50** can be connected to a required number of unit cells (**10** or **20**) in accordance with required characteristics of the diode element. Thus, a desired diodicity can be obtained by using arbitrary unit cells, which is advantageous in that designing the diode element can be easy.

When the N^+ diffusion region **12** of the first unit cell **10** and the P^+ diffusion region **22** of the second unit cell **20** are constituted so as to be as small in size as possible, the distance between the anode and the cathode can be decreased further. As a result, the parasitic resistance **40** can be reduced effectively. Moreover, also the size of the diode element **100** can be reduced and the chip area of a semiconductor device can be also reduced. Therefore, it is preferable that the dimension that defines the size of each of the N^+ diffusion region **12** and the P^+ diffusion region **22** (e.g., the length of each side of the square) is

substantially the same as the minimum dimension that is allowed by the design rule.

In this embodiment, when the minimum dimension that is allowed by the design rule for producing the N^+ diffusion region **12** and the P^+ diffusion region **22** is about 1.4μm, the dimension that defines the size of each of the N^+ diffusion region **12** and the P^+ diffusion region **22** is set to be substantially the same as that, for example, about 2μm. In other words, they are set to the optimum (the smallest) size in light of non-uniformity during the production process and the like.

The N^+ diffusion region **12** of the first unit cell **10** and the P^+ diffusion region **22** of the second unit cell **20** viewed from the normal line direction of the substrate are for example, square in shape. This is because, when the N^+ diffusion region **12** and the P^+ diffusion region **22** are set to be square in shape, the first unit cell **10** and the second unit cell **20** can be arranged most efficiently within the predetermined design rule. However, the N^+ diffusion region **12** and the P^+ diffusion region **22** are not required to be geometrically precise square, but it is sufficient that they are substantially square in shape. For example, they may have curved corners or the length of each side may not be precisely equal to each other. Moreover, the shape is not necessarily square and, for example, each of the N^+ diffusion region **12** and the P^+ diffusion region **22** may be regular hexagon in shape as in a honeycomb structure.

Furthermore, the N^+ diffusion region **12** and the P^+ diffusion region **22** can be also circular or elliptic in shape.

In addition, in this embodiment, the first unit cells **10** and the second unit cells **20** are arranged alternately. For example, they are arranged in a checkered pattern (or, for example, a pattern of a chessboard). When the first unit cells **10** and the second unit cells **20** are arranged in a checkered pattern, the distance between each of the first unit cells **10** and each of the second unit cells **20** can be decreased. Therefore, it is advantageous in that the parasitic resistance **40** can be reduced even if the plurality of first unit cells **10** and the plurality of second unit cells **20** are provided.

According to the structure of the diode **100**, voltage drop due to the parasitic resistance **40** can be reduced and the current capacity per unit area can be significantly improved. Moreover, since the N^+ diffusion region and the P^+ diffusion region that constitute a diode are constituted with the first unit cell **10** and the second unit cell **20**, respectively, circuit design can be performed based on the unit cell. Thus, an advantage of the improved convenience during design of a diode that has required characteristics (desired characteristics) can be obtained. Therefore, the diode element **100** can be preferably used, for example, as an element of a bandgap reference circuit in an analog circuit section.

Next, an example of methods for producing the diode

100 of this embodiment will be described with reference to FIGS. 2(a) to 2(e). The diode 100 is produced, for example, by using a typical CMOS process, and can be produced by using the same process as that for a digital circuit section of a semiconductor integrated circuit.

First, for example, a P-type semiconductor substrate (e.g., a P-type silicon substrate) 60 is prepared as shown in FIG. 2(a), and then, element isolation region oxide films 32 are selectively formed partially in the substrate 60 from the surface thereof to a predetermined depth as shown in FIG. 2(b).

Next, as shown in FIG. 2(c), an N-well region (NW) 30 is formed as a first conductive type semiconductor layer, for example, by ion-implantation. In this step, a P-well region 36 that is positioned around the N-well region 30 is also formed.

Next, as shown in FIG. 2(d), N^+ diffusion regions 12 (first unit cells 10) and P^+ diffusion regions 22 (second unit cells 20) are selectively formed partially in the N-well region 30. The N^+ diffusion regions 12 and the P^+ diffusion regions 22 may be formed, for example, by ion-implantation.

Next, as shown in FIG. 2(e), after depositing an insulating film 54 on the substrate 60, contact holes are formed selectively on the insulating film 54, and then, a line 50 (including contact sections 52) is formed. Since the contact sections 52 of the line 50 are joined to each of

the contact sections **12** of the first unit cells **10** and the contact sections **22** of the second unit cells **20**, each of the first unit cells **10** and the second unit cells **20** are electrically connected to the line **50**. Thus, the diode element **100** can be obtained.

In the diode element **100**, the element isolation region oxide film **32** is formed in the intercell region between the first unit cell **10** and the second unit cell **20**. However, it is also possible to constitute a diode element **200** in which a gate electrode structure **70** is formed on the intercell region as shown in FIGS. **3(a)** and **3(b)**, without forming the element isolation region oxide film **32**. The gate electrode structure **70** includes an insulating layer (e.g., a gate oxide film) **72** and a conductive layer (e.g., a polysilicon layer) **74** formed thereon, and has a structure that can be produced by using the typical CMOS process.

In the diode element **200** shown in FIG. **3**, the gate electrode structure **70** is provided on the intercell region, and thus the N^+ diffusion regions **12** of the first unit cells **10** and the P^+ diffusion regions **22** of the second unit cells **20** can be separated from each other without forming the element isolation region oxide film **32**. Therefore, in addition to the area of the bottom surfaces of the P^+ diffusion regions **22**, the area of the outer circumferential surfaces of the P^+ diffusion regions **22** can contribute to the area of the pn junction, so that the area of the pn junction can be increased. Moreover, the gate electrode

structures **70** can be formed with the CMOS process. This is of a great advantage in that the gate electrode structures **70** of the diode element **200** can be formed by using the same process as that of the analog circuit section.

Moreover, in the diode element **200**, a gate line (not shown) can be also electrically connected to the gate electrode structures **70** positioned on the N-well region **30**. When a gate line is provided in the gate electrode structures **70** and a voltage (Vdd) of the high potential side is applied to the gate line as an independent potential, it is possible to make it difficult to apply a reverse bias during a diode operation. Therefore, the formation of a depletion layer can be prevented, and as a result, a reduction in the area of the pn junction can be suppressed.

The diode element **200** can be produced as shown in FIGS. **4(a)** to **4(b)**, for example, by using the typical CMOS process. In this example, the diode element **200** having a structure in which a gate line **56** is formed on the gate electrode structure **70** is produced.

First, for example, a P-type semiconductor substrate (e.g., a P-type silicon substrate) **60** is prepared as shown in FIG. **4(a)**, and then, element isolation region oxide films **32** are selectively formed partially in the substrate **60** from the surface thereof to a predetermined depth as shown in FIG. **4(b)**. Unlike the example shown in FIG. **2**, it is unnecessary to form the element isolation region oxide film **32** in a portion that will be formed into an N-well region (NW) **30**,

because a gate electrode structure **70** will be formed in a subsequent step (see FIG. **4(d)**).

Next, as shown in FIG. **4(c)**, the N-well region (NW) **30** is formed as a first conductive type semiconductor layer, for example, by ion-implantation. In this step, a P-well region **36** that is positioned around the N-well region **30** is also formed.

Next, as shown in FIG. **4(d)**, the gate electrode structure **70** is formed in a portion that will be an intercell region between the first unit cell **10** and the second unit cell **20**. The formation of the gate electrode structure **70** can be performed, for example , as follows. First, after depositing an oxide film (e.g., oxide silicon (SiO_2)) on the substrate **60**, for example, polysilicon is deposited thereon. Then, both of them are selectively etched to form a gate oxide film (thickness: few nanometers) **72** and a conductive layer (polysilicon gate, thickness: several hundred nanometers) **74**. Thus, the gate electrode structure **70** is formed in the intercell region.

Next, as shown in FIG. **4(e)**, N^+ diffusion regions **12** (first unit cells **10**) and P^+ diffusion regions **22** (second unit cells **20**) are selectively formed partially in the N-well region **30** by using the gate electrode structures **70** as part of a mask. Since the gate electrode structures **70** are formed in the intercell region, the N^+ diffusion regions **12** and the P^+ diffusion regions **22** can be formed without damaging the diodicity even if the element isolation region

oxide film **32** is not formed in the N-well region **30**.

Next, as shown in FIG. **4(f)**, after depositing an insulating film **54** on the substrate **60**, contact holes are formed selectively in the insulating film **54**, and then a line **50** (including contact sections **52**) and a gate line **56** are formed. The contact sections **52** of the line **50** are joined to each of the contact sections **14** of the first unit cells **10** and the contact sections **24** of the second unit cells **20**. The gate line **56** is electrically connected to the conductive layer **74** of the gate electrode structure **70**. Thus, the diode element **200** can be obtained.

FIG. **5** shows a circuit for the voltage/current characteristics of a diode, and FIG. **6** shows the measurement results of the voltage/current characteristics of the diode measured with the circuit shown in FIG. **5**. The vertical axis in FIG. **6** shows the current per unit area (logarithmic scale) and the horizontal axis shows the applied voltage. The solid line in FIG. **6** shows the result obtained when the diode element **200** of the present invention is used, in which the voltage is not applied to the gate electrode structure **70** of the diode element **200**. On the other hand, the broken line in FIG. **6** shows the result obtained when the diode element **1000** (a comparative example)shown in FIG. **15** is used.

FIG. **6** indicates that at any applied voltage Vd within the operating range of a diode, the diode element **200** of the present invention shows more excellent characteristics than the diode element **1000**.

FIG. **7** shows an enlarged portion where the applied voltage is around 0.7V in the graph of FIG. **6**. As shown in FIG. **7**, when the applied voltage is 0.7V, the current per unit area of the diode element **200** is about 2.3 times higher than that of the diode element **1000** (the comparative example). In other words, it can be understood that the diode element **200** of the present invention has excellent characteristics.

FIG. **8** is a graph showing the range of 0.6V to 1.0V as the applied voltage in the graph of FIG. **6**, which is represented with a vertical axis with decimal scale. As can be understood from FIG. **8**, as the applied voltage becomes higher, the difference between the current capacity of the diode element **200** of the present invention and the current capacity of the diode element **1000** (the comparative example) increases because of the influence of the parasitic resistance of the N-well region. From these results, it can be understood that, in the diode element **200** of this embodiment, the current per unit area (a diode current ID) can be increased, while the influence of the parasitic resistance **40** of the N-well region **30** is suppressed to be as low as possible. In FIGS. **7** and **8**, "E-X" on the vertical axes means 10^{-X}, and for example, 1.0E-05[A] represents 1.0×10^{-5}[A].

(Embodiment **2**)

Embodiment **2** of the present invention will be

described with reference to FIGS. **9** and **10**. FIG. **9(a)** is a schematic top view showing a diode element **300** of a semiconductor device of this embodiment, and FIG. **9(b)** is a schematic cross-sectional view of the diode element **300** taken along line **b-b'** of FIG. **9(a)**.

The diode element **300** of this embodiment is different from the diode elements **100** or **200** of Embodiment **1** that are formed in the N-well region **30**, in that it is formed in a semiconductor region of an SOI (silicon on insulator) substrate. In other words, this embodiment uses a first conductive type semiconductor layer (semiconductor region) **30** formed on an insulating film (or an insulating substrate) **62** as the first conductive type semiconductor layer. The first conductive type semiconductor layer **30** may be an N-type semiconductor layer or a P-type semiconductor layer. For simplification of description of this embodiment, hereinafter (including the following embodiments), the aspects different from those in Embodiment **1** will be mainly described, and description of the same aspects are either omitted or simplified.

A diode element **300** includes first unit cells **10** and second unit cells **20** in a first conductive type semiconductor layer **30** (thickness: e.g., about 5nm) that is formed on an insulating film (for example, a buried oxide film, thickness: e.g., about 100nm) **62**. A gate electrode structure **70** is formed in an intercell region between the first unit cell **10** and the second unit cell **20**. The gate

electrode structure **70** can be provided with a gate line (not shown). In this embodiment, an oxide film **64** for isolating elements is formed around the semiconductor layer **30**, and a P-type semiconductor substrate is positioned under the insulating film (the buried oxide film) **62**. Moreover, as well as Embodiment **1** described above, the first unit cells **10** and the second unit cells **20** are arranged in a checkered pattern in the semiconductor region **30**.

In the diode element **300**, N^+ diffusion regions **12** of the first unit cells **10** and P^+ diffusion regions **22** of the second unit cells **20** are formed in the semiconductor region (semiconductor layer **30**) of the SOI substrate where the N-well region and the P-well region are not formed. Therefore, the area of the outer circumferential surface of each of the N^+ diffusion regions **12** and the P^+ diffusion regions **22** contributes to the area of the pn junction, so that the area of the pn junction can be increased. As a result, the current capacity of the diode element can be improved. Moreover, in the structure of the diode element **300** as well as in the case of the above embodiment, the first unit cells **10** and the second unit cells **20** can be arranged in close proximity to each other so that a parasitic capacitance **40** of the semiconductor layer **30** can be reduced.

The diode element **300** can be produced, for example, as shown in FIGS. **10(a)** to **10(f)**. In this example, a diode element including a gate line **56** that is formed on a gate electrode structure **70** is produced.

First, as shown in FIG. **10(a)**, for example, an SOI substrate provided with a buried oxide layer (SiO_2 film) **62** on a P-type semiconductor substrate (a P-type silicon substrate) **60** and a semiconductor region (a semiconductor layer) **30** formed thereon is prepared.

Next, as shown in FIG. **10(b)**, an insulating film **64** for isolating elements is selectively formed partially in the semiconductor region **30** of the SOI substrate, and then a gate electrode structure **70** is formed in a portion that will be an intercell region between the first unit cell **10** and the second unit cell **20** as shown in FIG. **10(c)**.

Next, as shown in FIG. **10(d)**, N^+ diffusion regions **12** (first unit cells **10**) and P^+ diffusion regions **22** (second unit cells **20**) are selectively formed partially in the semiconductor layer **30** by using the gate electrode structures **70** as part of a mask. When the SOI substrate is used as in this embodiment, a method of forming the gate electrode **70** without forming an element isolation region oxide film is more preferable in the production process than a method of forming the element isolation region oxide film **32** as in the diode element **100** of Embodiment **1** described above.

Next, as shown in FIG. **10(f)**, after depositing an insulating film **54** on the SOI substrate, contact holes are formed selectively in the insulating film **54**, and then, a line **50** (including contact sections **52**) and a gate line **56** are formed. Thus, the diode element **300** can be obtained.

(Embodiment 3)

Embodiment 3 of the present invention will be described with reference to FIGS. 11 to 13. In the above embodiments, a diode element is constituted by using the first unit cells 10 and the second unit cells 20, but it is also possible to constitute a bipolar transistor element by utilizing this constitution. FIG. 11(a) is a schematic top view showing the bipolar transistor element 400 included in a semiconductor device of this embodiment, and FIG. 11(b) is a schematic cross-sectional view of the bipolar transistor element 400 taken along line b-b' of FIG. 11(a).

As shown in FIGS. 11(a) and 11(b), the bipolar transistor element 400 can be constituted by using the first unit cell 10, the second unit cell 20 and a P-type semiconductor substrate (a second conductive type semiconductor layer) 60 in the structure of the diode element 100 of Embodiment 1 as a base, an emitter and a collector, respectively. FIG. 12 is another schematic view showing the bipolar transistor element 400 for further clarification of the relationship among the base (B), the emitter (E) and the collector (C).

In the bipolar transistor element 400 shown in FIG. 11, a line 50a for the emitter is electrically connected to a contact region 24 of the second unit cell 20, and a line 50b for the base is electrically connected to a contact region 14 of the first unit cell 10. A line 50c for the collector

is electrically connected to a P+ diffusion region **34** formed in a P-well region **36** adjacent to an N-well region **30**, whereby the line **50c** for the collector and the P-type semiconductor substrate **60** are electrically connected to each other.

In the bipolar transistor element **400**, either of the first unit cell **10** or the second unit cell **20** is used as the base (B) or the emitter (E). As is explained in the above embodiments, since the first unit cells **10** and the second unit cells **20** can be arranged in close proximity to each other, the parasitic resistance **40** of the N-well region **30** can be reduced. As a result, a bipolar transistor element having excellent current characteristics can be provided. In the structure shown in FIG. **11**, the element isolation region oxide films **32** are provided between the first unit cells **10** and the second unit cells **20**. However, it is of course possible to provide a gate electrode structure **70** in the intercell region without providing the element isolation region oxide film **32**.

Furthermore, as shown in FIG. **13**, it is also possible to constitute a bipolar transistor element **450** with a double-well type structure. More specifically, an N-well region **31** is formed in the P-type semiconductor substrate **60** as a second conductive type semiconductor layer, and a P-well region **30** is formed in the N-well region **31** as a first conductive type semiconductor layer. In such a double-well type structure, a bipolar transistor element can be

constituted by providing the first unit cell (the base) **10** and the second unit cell (the emitter) **20** in the P-well region **30** as the first conductive type semiconductor layer, and using the N-well region as the collector. Even in this structure as well as in the bipolar transistor element **400**, the parasitic resistance of the P-well region **30** can be reduced, so that a bipolar transistor having excellent current characteristics can be provided.

(Embodiment **4**)

Embodiment **4** of the present invention will be described with reference to FIG. **14**. In the foregoing embodiments, the first unit cells **10** and the second unit cells **20** are arranged in a checkered pattern (e.g., see FIG. **1**) in order to arrange the first unit cells **10** and the second unit cells **20** alternately in the first conductive type semiconductor layer **30**. However, in this embodiment, a comparatively large first unit cell **10** is formed in the first conductive type semiconductor layer **30**, and second unit cells **20** are formed in the first unit cell **10**.

FIG. **14(a)** is a schematic top view showing a diode element **500** included in a semiconductor device of this embodiment, and FIG. **14(b)** is a schematic cross-sectional view of the diode element **500** taken along line **b-b'** of FIG. **14(a)**. The diode element **500** includes a first unit cell **10** in a first conductive type semiconductor layer (N-well) **30** and a plurality of second unit cells **20** formed in the first

unit cell **10**. In this embodiment, the first unit cell **10** viewed from the normal line direction of the substrate is for example, square in shape (the length of each side: about 5μm), and the second unit cells **20** are also square in shape (the length of each side: about 25μm). For example, four second unit cells **20** are formed in the first unit cell **10**. A spacing **15** between the first unit cell **10** and the second unit cells **20** is for example, about 2μm.

Even in the structure of the diode element **500**, the distance from the center of an N^+ diffusion region **12** serving as a cathode to a P^+ diffusion region **22** serving as an anode can be shorter than that in the structure of the diode element **1000** shown in FIG. **15**. Therefore, the parasitic resistance of the first conductive type semiconductor layer (the N-well region) **30** can be reduced, so that a diode element having an improved current capacity per unit area can be provided.

Industrial Applicability

According to the present invention, a semiconductor device including a high-performance diode element that occupies only a small area can be provided. Since the high-performance diode element that occupies only a small area can be used preferably, for example, as an element of an analog circuit section of an analog/digital mixed LSI that is realized by a CMOS process, a semiconductor device having higher-performance and a smaller chip area can be provided.

CLAIMS

1. A semiconductor device comprising:

a first conductive type semiconductor layer;

at least one first unit cell including a first conductive type first semiconductor region formed in the first conductive type semiconductor layer and a contact region for electrically connecting the first semiconductor region to a line; and

at least one second unit cell including a second conductive type second semiconductor region formed in the first conductive type semiconductor layer and a contact region for electrically connecting the second semiconductor region to a line,

wherein the first unit cell and the second unit cell act as a diode element in cooperation.

2. The semiconductor device according to claim 1,

wherein the at least one first unit cell is a plurality of first unit cells and the at least one second unit cell is a plurality of second unit cells.

3. The semiconductor device according to claim 1 or 2,

wherein a dimension that defines a size of each of the first semiconductor region and the second semiconductor region is substantially a same as a minimum dimension that is allowed by a design rule for the semiconductor device.

4. The semiconductor device according to any of claims 1 to 3,

wherein each of the first semiconductor region and the second semiconductor region viewed from a normal line direction is substantially square in shape.

5. The semiconductor device according to any of claims 1 to 4,

wherein the first unit cells and the second unit cells are arranged in a checkered pattern in the first conductive type semiconductor layer.

6. The semiconductor device according to any of claims 1 to 5,

wherein the first unit cell and the second unit cell are arranged in the first conductive type semiconductor layer with a predetermined distance to each other, and

on an intercell region that is positioned between the first unit cell and the second unit cell in the first conductive type semiconductor layer, a gate electrode structure including at least an insulating layer formed on the cell region and a conductive layer formed on the insulating layer is formed.

7. The semiconductor device according to claim 6, further comprising a gate line electrically connected to the gate

electrode structure.

8. The semiconductor device according to claim 1,

wherein a plurality of second unit cells are formed in the first semiconductor region of one first unit cell.

9. The semiconductor device according to any of claims 1 to 8, further comprising a second conductive type semiconductor layer,

wherein the first conductive type semiconductor layer is formed on the second conductive type semiconductor layer.

10. The semiconductor device according to claim 9,

wherein the first unit cell formed in the first conductive type semiconductor layer is used as a base, and the second unit cell is used as an emitter, and the second conductive type semiconductor layer is used as a collector.

11. The semiconductor device according to claim 9 or 10,

wherein the second conductive type semiconductor layer is a semiconductor substrate, and

the first conductive type semiconductor layer is a well region formed in the semiconductor substrate.

12. The semiconductor device according to any of claims 1 to 8,

wherein the first conductive type semiconductor layer

is formed on an insulating layer.

13. The semiconductor device according to any of claims 1 to 12, further comprising an analog circuit section and a digital circuit section,

wherein the diode element is formed in the analog circuit section, and

the analog circuit section and the digital circuit section are produced by a CMOS process.

FIG. 1

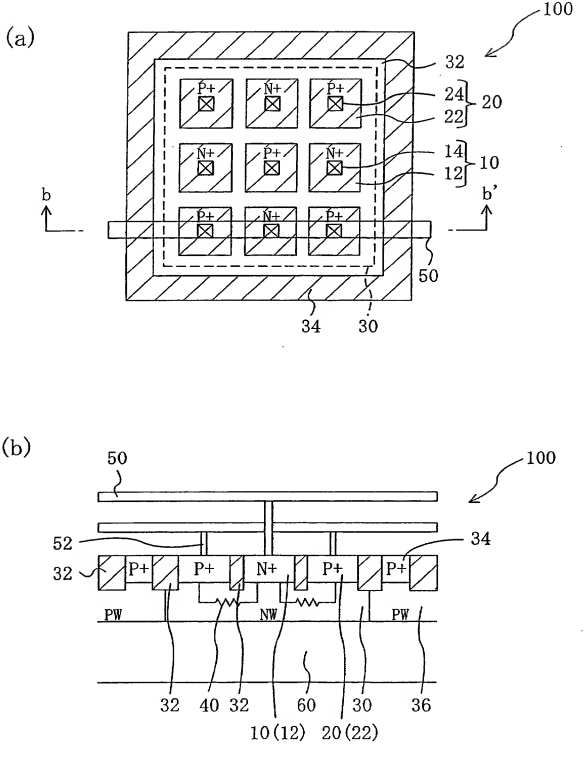

(a)
100
32
24
22
20
14
12
10
b
b'
50
34
30
(b)
50
100
52
34
32
P+
P+
N+
P+
P+
PW
NW
PW
32
40
32
60
30
36
10(12)
20(22)

FIG. 2

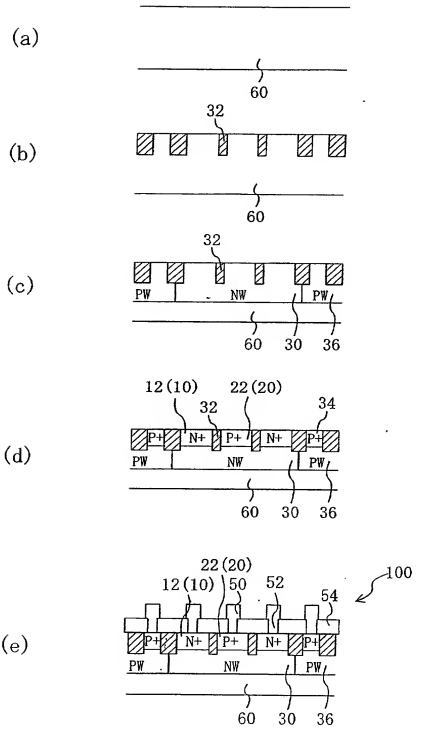


FIG. 3

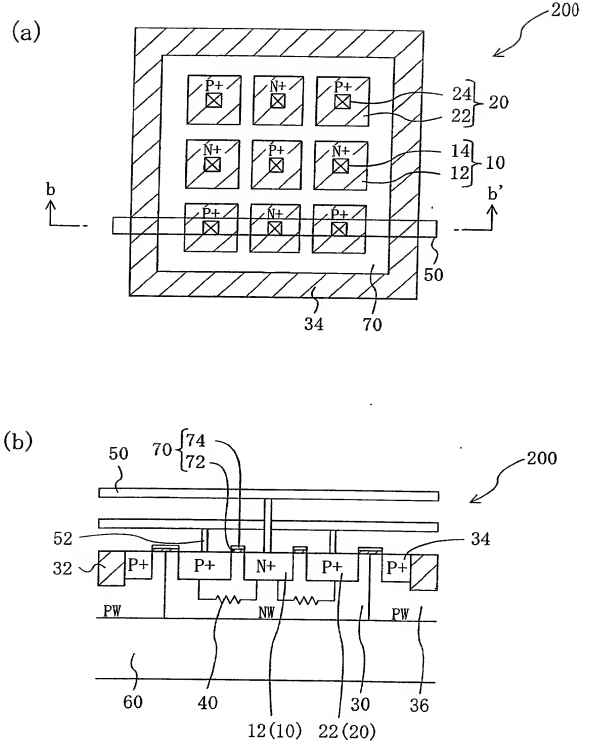
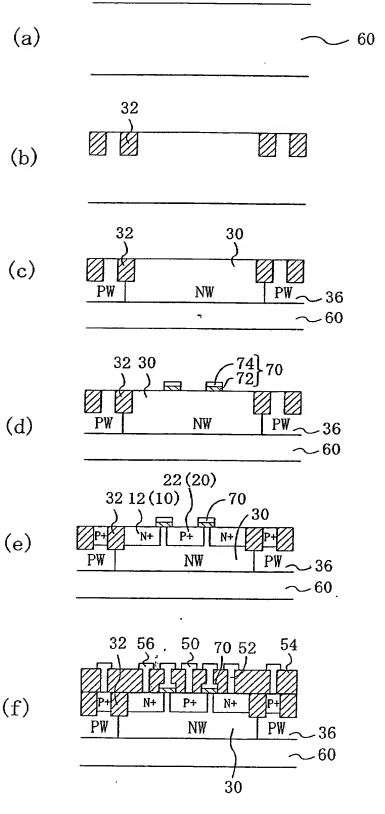

(a)
200
P+
N+
24
22
20
14
12
10
b
b'
50
34
70
(b)
50
70
74
72
200
52
34
32
PW
NW
60
40
12(10)
22(20)
30
36

FIG. 4


(a)
60
(b)
32
(c)
32
30
PW
NW
PW
36
60
(d)
32 30
74
72
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PW
NW
PW
36
60
(e)
22 (20)
32 12 (10)
70
30
P+
N+
P+
N+
P+
PW
NW
PW
36
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NW
PW
36
60
30

FIG. 5

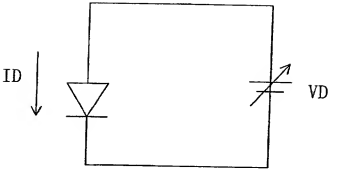

ID
VD

FIG. 6

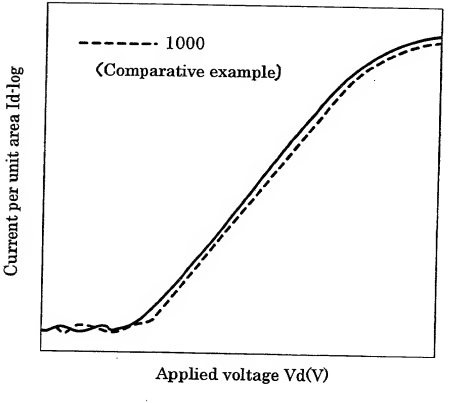

1000
(Comparative example)
Current per unit area Id-log
Applied voltage Vd(V)

FIG. 7

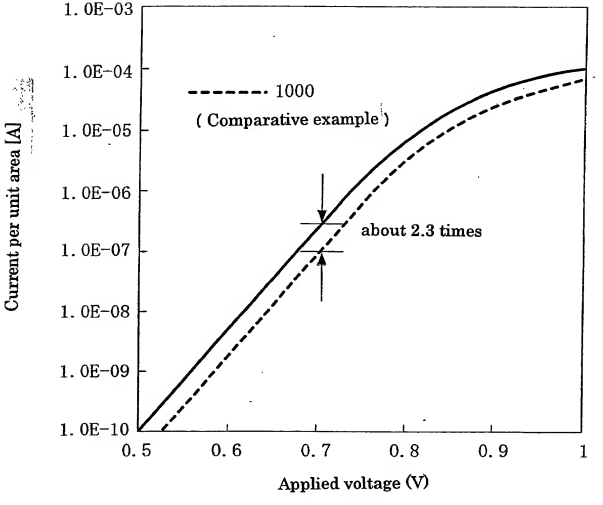

1. 0E-03
1. 0E-04
1. 0E-05
1. 0E-06
1. 0E-07
1. 0E-08
1. 0E-09
1. 0E-10
Current per unit area [A]
1000
(Comparative example)
about 2.3 times
0. 5
0. 6
0. 7
0. 8
0. 9
1
Applied voltage (V)

FIG. 8

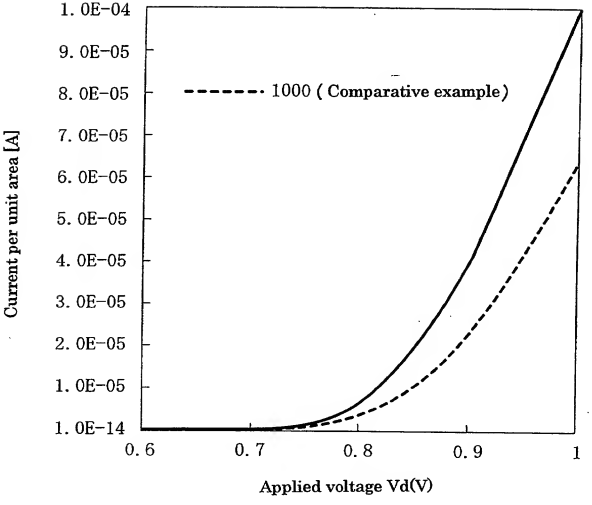

1. 0E-04
9. 0E-05
8. 0E-05
7. 0E-05
6. 0E-05
5. 0E-05
4. 0E-05
3. 0E-05
2. 0E-05
1. 0E-05
1. 0E-14
1000 (Comparative example)
Current per unit area [A]
0. 6
0. 7
0. 8
0. 9
1
Applied voltage Vd(V)

FIG. 9

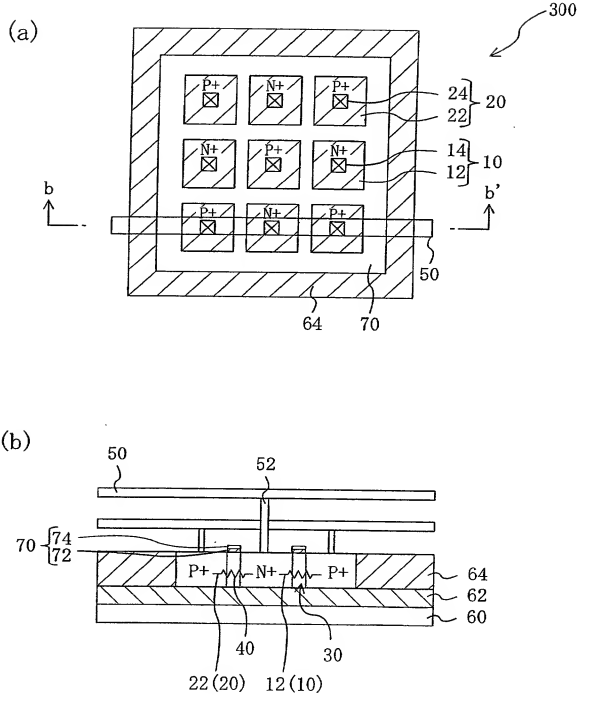

(a)
300
P+
N+
24
22
20
14
12
10
b
b'
50
64
70
(b)
50
52
70
74
72
P+
N+
P+
64
62
60
40
30
22(20)
12(10)

FIG. 10

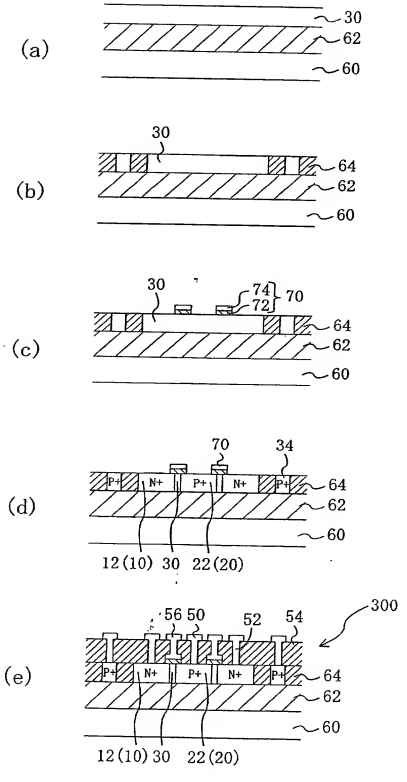

(a)
30
62
60
(b)
30
64
62
60
(c)
30
74
72
70
64
62
60
(d)
70
34
P+
N+
P+
N+
P+
64
62
60
12(10)
30
22(20)
(e)
56
50
52
54
300
P+
N+
P+
N+
P+
64
62
60
12(10)
30
22(20)

FIG. 11

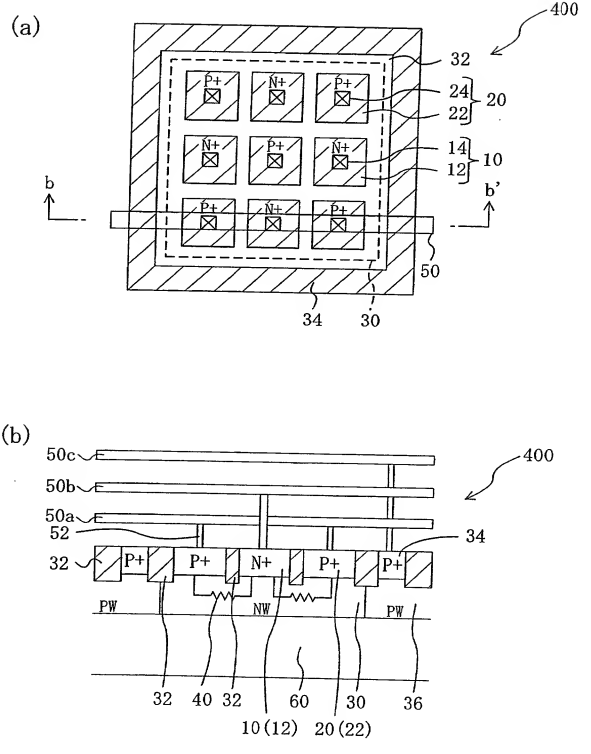

(a)
400
32
24
22
20
14
12
10
b
b'
50
34
30
P+
N+
(b)
50c
50b
50a
52
34
32
PW
NW
32
40
32
60
30
36
10(12)
20(22)

FIG. 12

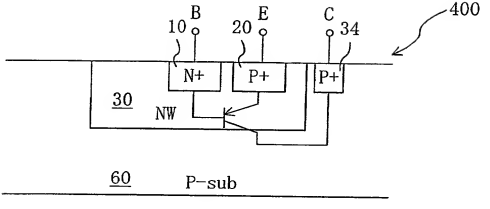

B
E
C
10
20
34
400
N+
P+
P+
30
NW
60
P-sub

FIG. 13

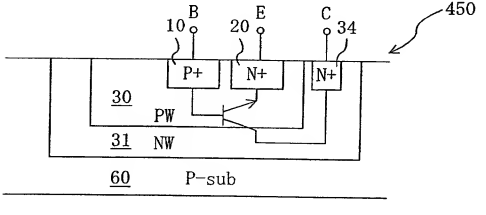

B
E
C
10
20
34
450
P+
N+
N+
30
PW
31
NW
60
P-sub

FIG. 14

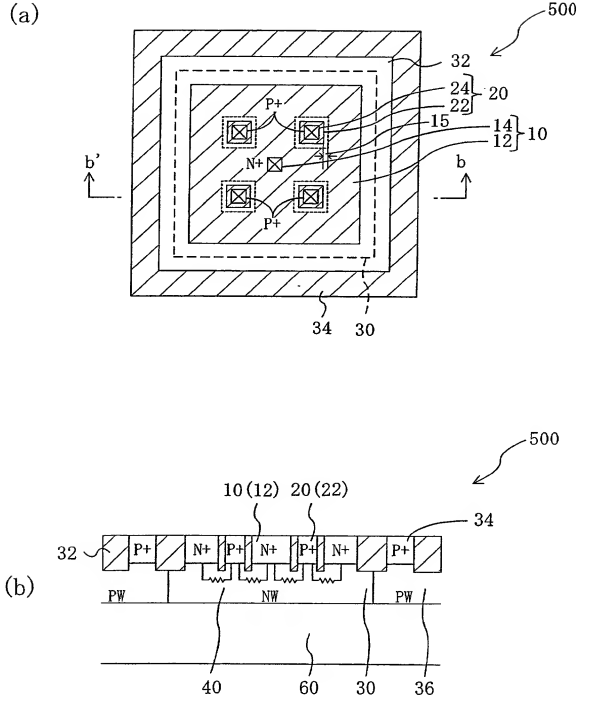
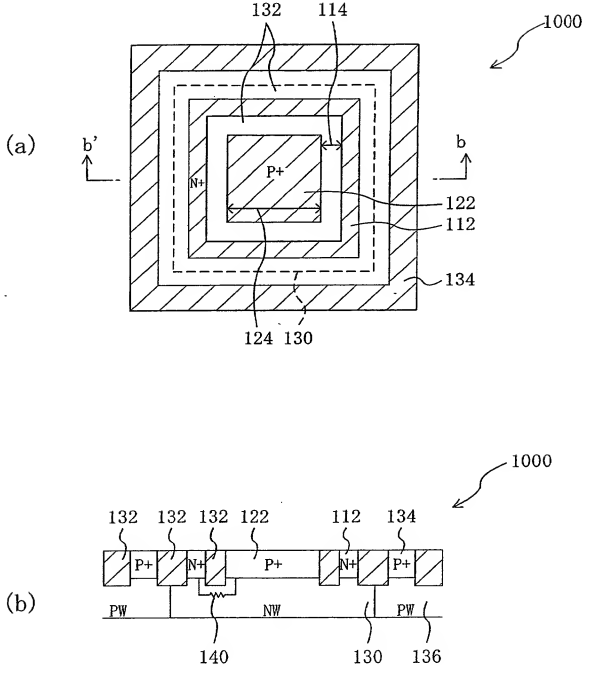

(a)
500
32
24
22
20
15
14
12
10
P+
N+
b'
b
34
30
(b)
500
10(12)
20(22)
34
32
P+
N+
PW
NW
40
60
30
36

FIG. 15


(a)
132
114
1000
b'
b
N+
P+
122
112
134
124
130
(b)
1000
132
132
132
122
112
134
P+
N+
P+
N+
P+
PW
NW
PW
140
130
136

Docket No. _____

COMBINED DECLARATION/POWER OF ATTORNEY FOR PATENT APPLICATION

As a below named inventor(s), I (we) hereby declare that:

My residence, post office address and citizenship are as stated below next to my name.

I believe I am the original, first and sole inventor (if only one name is listed below) or an original, first and joint inventor (if plural names are listed below) of the subject matter which is claimed and for which a patent is sought on the invention entitled

SEMICONDUCTOR DEVICE

_____, the specification of which

(check one)

___ is attached hereto.

___ was filed on _____ as United States Application No. _____.

__X__ PCT International Patent Application Number **PCT/JP00/03884** filed on **June 14, 2000** and was amended on _____ (if applicable).

I hereby state that I have reviewed and understand the contents of the above identified specification, including the claims, as amended by any amendment referred to above.

I acknowledge the duty to disclose information which is material to the examination of this application in accordance with Title 37, Code of Federal Regulations, § 1.56(a).

I hereby claim foreign priority benefits under Title 35, United States Code, § 119 of any foreign application(s) for patent or inventor's certificate listed below and have also identified below any foreign application for patent or inventor's certificate having a filing date before that of the application on which priority is claimed:

Prior Foreign Application(s)			Priority Claimed
11-169251 (Number)	JAPAN (Country)	16/06/1999 (Day/Month/Year Filed)	X Yes __ No
_____ (Number)	_____ (Country)	_____ (Day/Month/Year Filed)	__ Yes __ No
_____ (Number)	_____ (Country)	_____ (Day/Month/Year Filed)	__ Yes __ No

I hereby claim the benefit under Title 35,United States Code, § 120 of any United States application(s) listed below and, insofar as the subject matter of each of the claims of this application is not disclosed in the prior United States application in the manner provided by the first paragraph of Title 35, United States Code, § 112, I acknowledge the duty to disclose material information as defined in Title 37, Code of Federal Regulations, § 1.56(a) which occurred between the filing date of the prior application and the national or PCT international filing date of this application:

(Appln. Serial No.)	(Filing Date)	(Status-patented, pending, abandoned)
(Appln. Serial No.)	(Filing Date)	(Status-patented, pending, abandoned)

(13) I hereby appoint as my attorneys, with full power of substitution and revocation, to prosecute the patent application identified above and to transact all business in the U.S. Patent and Trademark Office connected therewith: Raphael V. Lupo (Reg. No. 28,363); Jack Q. Lever, Jr. (Reg. No. 28,149); Kenneth L. Cage (Reg. No. 26,151); Stanislaus Aksman (Reg. No. 28,562); Michael E. Fogarty (Reg. No. 36,139); Brian E. Ferguson (Reg. No. 36,801); Robert W. Zelnick (Reg. No. 36,976); Edward E. Kubasiewicz (Reg. No. 30,020); Paul Devinsky (Reg. No. 28,553); and Wilhlem F. Gadiano (Reg. No. 37,136); Laura A. Donnelly (Reg. No. 38,435); Craig L. Plastrik (Reg. No. 41,254), David A. Spenard (Reg. No. 37,449)

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I hereby declare that all statements made herein of my own knowledge are true and that all statements made on information and belief are believed to be true; and further that these statements were made with the knowledge that willful false statements and the like so made are punishable by fine or imprisonment, or both, under Section 1001 of Title 18 of the United States Code and that such willful false statements may jeopardize the validity of the application or any patent issued thereon.

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